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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/812,923	03/31/2004	Takeshi Ichikawa	030712-34	5693	
22204	7590 04/06/2005	·	EXAM	EXAMINER	
NIXON PEABODY, LLP 401 9TH STREET, NW		CUNNINGHAM, TERRY D			
SUITE 900	·		ART UNIT	PAPER NUMBER	
WASHINGTON, DC 20004-2128			2816		
			DATE MAILED: 04/06/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)

Paper No(s)/Mail Date 3/31/04.

Paper No(s)/Mail Date. ___

6) Other:

5) Notice of Informal Patent Application (PTO-152)

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Crocker et al. (3083907). Crocker et al. discloses, in Figs. 1 and 2, a circuit comprising: an "input means (12)"; a "pulse generating means (the first gate 15, connected to A)"; "a plurality of modules (A-G)" including "a first control means" having a "first detection means (34 and 36 of module A of Fig. 2)" and "means for generating the first reset signal (30 and 32 of module A of Fig. 2)" and "a second control means" having a "second detection means (34 and 36 of module B of Fig. 2)" and "means for generating the second reset signal (30 and 32 of module B of Fig. 2)", all connected and operating similarly as recited by Applicant.

Claims 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al. (USPN 5,164,970). Shin et al. disclose, in Fig. 1A, a circuit comprising: "reset input means (LP and A3)"; "clock input means (A1)"; "clock control means (2, 3, 4 and 8)"; "a plurality of modules (26-30)"; and "a plurality of delay means (15-21)", all connected and operating similarly as recited by Applicant.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 571-272-1742. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 57,1-272-1740. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TC April 4, 2005 Terry D. Cunningham Primary Examine

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